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Implementation of Energy-Efficient Low Power 10T Full-Adder

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Abstract

In this Paper, the performance of 10-tranistor based full adder is analyzed and compared with that of two different types of full adder based on Swing Restored Complementary pass transistor (SR-CPL) XOR/XNOR logic gate and Double pass transistor logic (DPL) based CMOS Full Adder is designed using Tanner EDA Tool based up on 0.25µm CMOS Technology. As part of this we have performed the simulation of CMOS full adder using T-SPICE and BSIM3v31 tools of Tanner EDA. The parameters of power consumption, Area, Propagation Delay, and Power Delay Product (PDP) are evaluated to analyze the proposed Low Power full adder.

Keywords: SR-CPL, DPL, XNOR, CMOS, Tanner

Introduction

In the past periods, The technology has played an increasingly important role in integrated circuit industry was Complementary Metal Oxide Silicon (CMOS).This Concept made implementation in thin film transistor technology possible. In the beginning, only three circuits were implemented are not inverter, NOR gate and NAND gate. In order to implement of this circuits F.Wanlass built an nMOS transistor as pMOS transistors were only available at that time. After, these circuits are in the market because of their low power dissipation. In the beginning CMOS was applied to general system designs. Since the processing technology required in the implementation of CMOS circuits was complex.

In the CMOS there are complementary and Symmetrical pairs which are of P-type (PMOS) and N-Type (NMOS) which are used for implementation of logic functions. In a PMOS transistor we can have input from voltage source or from other PMOS transistor. NMOS transistor can have input from ground or other NMOS transistor. The scaling of Complementary Metal Oxide Semiconductor (CMOS) transistors has so far provided lower cost and higher performance circuits. The most important effects are the increase in power consumption and the decrease in reliability. CMOS logic is used in integrated Circuit, microprocessors, microcontrollers and other digital logic circuits for to reduce power consumption and being more immune towards noise occurring conditions.

The power-delay product (PDP) metric relates the amount of energy spent during the realization of determined task, and it stands for the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies.

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific and digital signal processing (DSP) architectures and microprocessors. The PDP exhibited by the full-adder would affect the system's overall performance [2]. Thus, the taking this fact into consideration of the design in a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems.

In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, and based on the multiplexing of the Boolean functions of DPL and SR-CPL, to obtain balanced delays in SUM and Carry outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption[6]. Two new full-adders have been designed using the existing logic structure. They are Double pass-transistor logic (DPL) Swing restored Complementary pass-transistor logic (SR-CPL). In the DPL style both NMOS and PMOS logic networks are used in parallel and this provides full swing on the output signals. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

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CPL is a static gate, because outputs are connected to Vdd or GND through a low-resistance path. Power dissipation is the most critical parameter or portability & mobility and it is classified in to dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation

It becomes an issue when the circuit is inactive or is in a power-down mode. There are three which are summarized in equation given below.

$$Pavg = \text{Pswitching} + Pshort - circuit + Pleakage = (\alpha_{0-1} \times C_L \times V_{dd}^2 \times F_{dk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd})$$

The first term represents the switching component overpower, where L C is the load capacitance, *clk*. f is the clock frequency and is the probability that a power consuming transition occurs (the activity factor). The second term due to the direct-path short circuit current, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, *leakage I* which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations.

Previous Work

Many papers have been published regarding the optimization of low-power full-adders, trying different options for the logic style Complementary pass-transistor logic (CPL), double pass-transistor logic (DPL), swing restored CPL (SR-CPL) , and hybrid styles and the logic structure used to build the adder module. The enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate.

The Figure 1 shows CPL schematic, the simulation of this environment has been used for compiling full adders' analyses within the addition of the inverters at the outputs. The size of the input buffers are degradation in the input signals, and the size of the output buffers equals to the load of 4 small inverters for this technology.

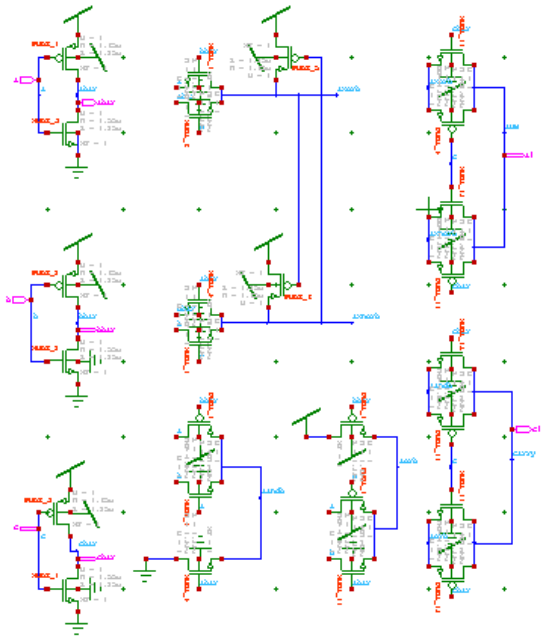

Figure 1: Schematic design of SR-CPL logic Structure

The main advantage of using the simulation environment is followed by the power consumption the energy required to charge and discharge to the internal nodes when the module have no direct power supply connections in case of pass transistors logic styles. The main importance of cpl and dpl are it effects the Power consumption which connects the input and output of device under test.

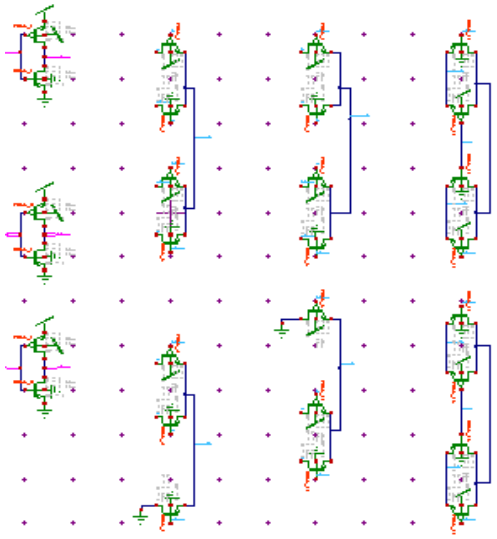

Figure 2: Schematic design of DPL logic Structure

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Existing Method

In the previous section the design is performed using schematic entry, and the same design is developed in the layout format. In this simulation the full adder performance and comparisons regarding area, power consumption, propagation delay and PDP. It consists of full adders with 2.5V source, pMOS and nMOS transistors are with 1.65mm and 0.55mm width. The Figure 3 shows the proposed CPL layout design.

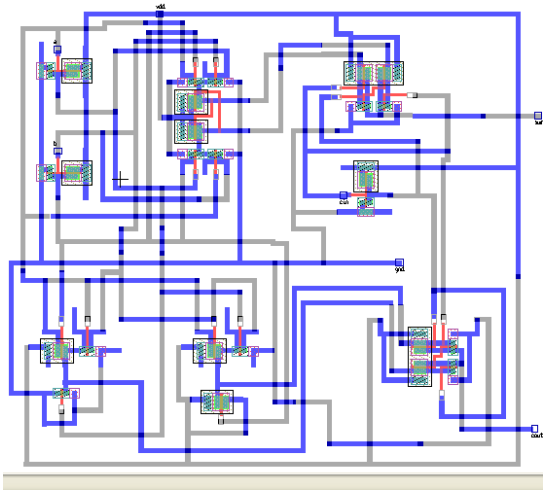

Figure 3: Layout designed of SR-CPL logic Structure

The Figure 4 shows DPL layout design which consists of 26 transistors and this layout is designed for determining lowest power supply voltage, which each full adder can tolerate.

In the short circuit consumption optimization related to power configuration of the constitute AND/OR gates and the dynamic consumption optimization comes from the reduced capacitance in the internal nodes of logic style. The PDP parameter defines the energy efficiency for the full adder to built new internal logic structure.

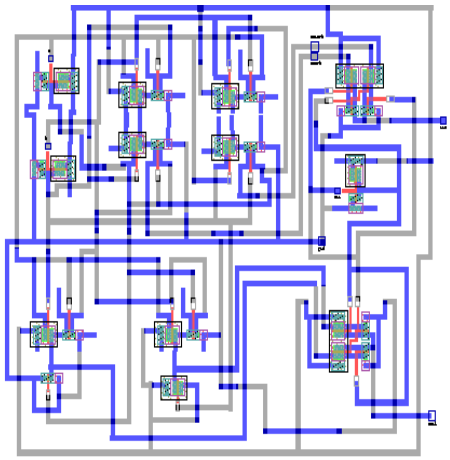

Figure 4: Layout designed of DPL logic Structure

In the present implementation, area obtained from the layouts. It can be seen that proposed full adders require the smallest area which can be considered as some factors for presenting delay and power consumption as it implies smaller parasitic capacitance being driven inside the full adder.

Proposed Work

The proposed work is implementation of 10T full adder. By which exhibit static dissipation and this is the new 10T and CPL adder which are implemented with logic style that have in-complement voltage swing resorted in some internal nodes, causing this consumption component. Which it was reduce Power delay product, Power, Area and dealy.The power consumption improves the full adder taken in descending order with optimizations power.

By using XNOR Based full adder it can provide low power with very efficiently optimizes its area. The implementation of this area obtained from layouts, it has been proposed for full adders requires the smallest area, which can also be considered has one factor for presenting low power consumption and delay for it implies smaller parasitic capacitance has been driven inside the full adder. The main reason for the smaller area compared to the other full adder that has been less transistors, is that size of the transistors in the proposed full adder.

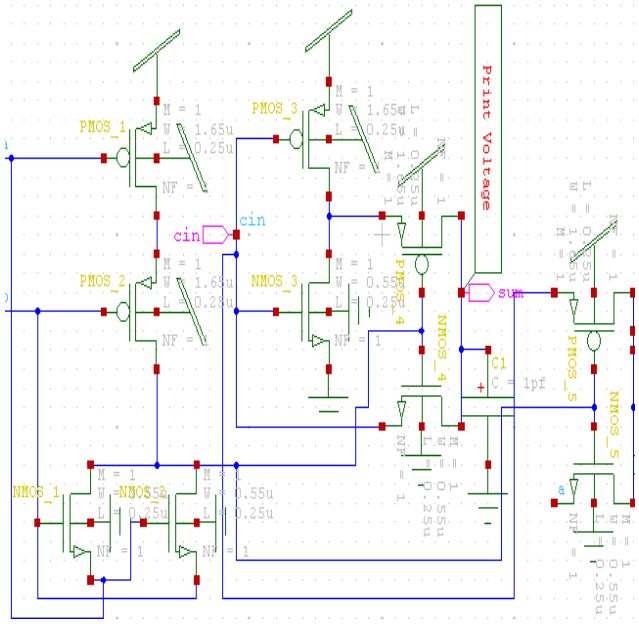

Figure 5: Schematic designed of 10 Transistor logic Structure

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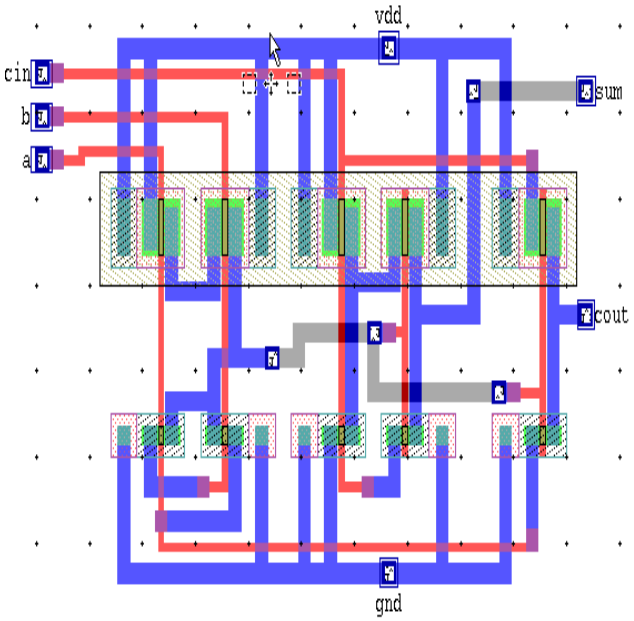
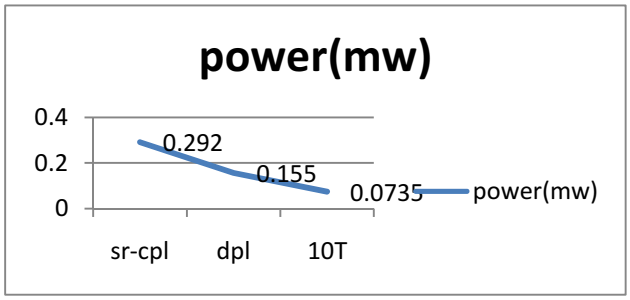


Figure 6: Layout designed of 10 Transistor logic Structure

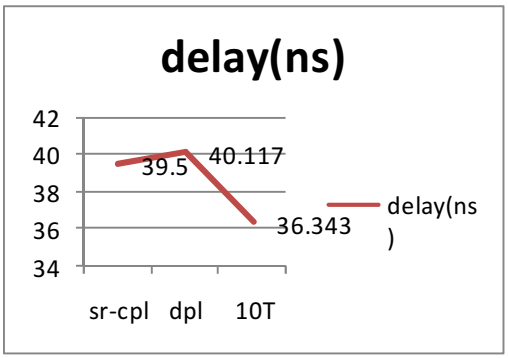
Simulation Result

By using S-Edit and L-Edit we have to calculate Power, Delay, Area and Power Delay Product (PDP). Considering the stimulation results the average delay for CPL is 39.5ns and for DPL is 40.117ns for comparing both when proposed work 10transistor has the average delay is 36.343ns.The average Power for CPL 0.292mw and DPL has 0.155mw, by comparing the power proposed work has 0.0735mw. The PDP for SR-CPL is 11.534pj and for DPL is 6.218pj for comparing both when proposed work 10transistor has the PDP is 2.6712pj.By using these values we have change in schematic capacitor values has Cl=1pF, Vdd=2.5v.

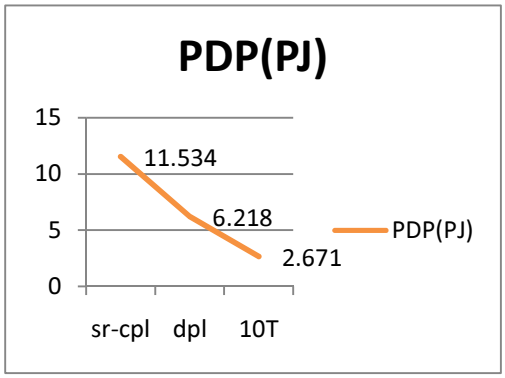
A. Power chart:



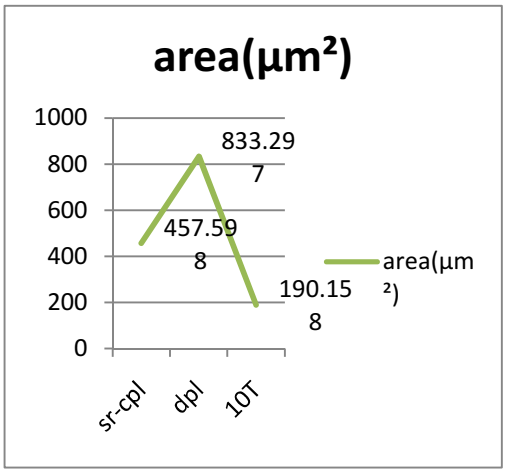
B. Delay chart:



C. PDP chart:



D. Area chart:



Conclusion

The paper presents design and implementation of XNOR Based full adder using fully static logic design style which is most suitable for low-energy applications. Also the realization of CMOS full adder gives even better calculation of Power Delay Product by using 0.25µm CMOS technology.

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